STRAINED SILICON MOSFETS HAVING IMPROVED THERMAL DISSIPATION

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates generally to fabrication of metal oxide semiconductor field effect transistors (MOSFETs), and, more particularly, to MOSFETs that achieve improved carrier mobility through the incorporation of strained silicon.

2. Related technology

[0002] MOSFETs are a common component of integrated circuits (ICs). Figure 1 shows a cross sectional view of a conventional MOSFET device. The MOSFET is fabricated on a silicon substrate 10 within an active region bounded by shallow trench isolations 12 that electrically isolate the active region of the MOSFET from other IC components fabricated on the substrate 10.

[0003] The MOSFET is comprised of a gate 14 and a channel region 16 that are separated by a thin gate insulator 18 such as silicon oxide or silicon oxynitride. A voltage applied to the gate 14 capacitively controls the creation of an inversion layer in the channel region 16 that provides carriers for conduction between the source and drain. To minimize the resistance of the gate 14, the gate 14 is typically formed of a doped semiconductor material such as polysilicon.

[0004] The source and drain of the MOSFET comprise deep source and drain regions 20 formed on opposing sides of the channel region 16. The deep source and drain regions 20 are formed by ion implantation subsequent to the formation of a spacer 22 around the gate 14. The spacer 22 serves as a mask during implantation to define the lateral positions of the deep source and drain regions 20 relative to the channel region 16.

[0005] Source and drain silicides 24 are formed on the deep source and drain regions 20 to provide ohmic contacts and reduce contact resistance. The silicides 24 are comprised of the substrate semiconductor material and a metal such as cobalt (Co) or nickel (Ni). The deep source and drain regions 20 are

formed deeply enough to extend beyond the depth to which the source and drain silicides 24 are formed. The gate 14 likewise has a silicide 26 formed on its upper surface. A gate structure comprising a polysilicon material and an overlying silicide is sometimes referred to as a polycide gate.

[0006] The source and drain of the MOSFET further comprise shallow source and drain extensions 28. As dimensions of the MOSFET are reduced, short channel effects resulting from the small distance between the source and drain cause degradation of MOSFET performance. The use of shallow source and drain extensions 28 rather than deep source and drain regions near the ends of the channel 16 helps to reduce short channel effects. The shallow source and drain extensions 28 are implanted after the formation of a protective layer 30 around the gate 14 and over the substrate, and prior to the formation of the spacer 22. The gate 14 and the protective layer 30 act as an implantation mask to define the lateral position of the shallow source and drain extensions 28 relative to the channel region 16. Diffusion during subsequent annealing causes the shallow source and drain extensions 28 to extend slightly beneath the gate 14.

[0007] One option for increasing the performance of MOSFETs is to enhance the carrier mobility of the MOSFET semiconductor material so as to reduce resistance and power consumption and to increase drive current, frequency response and operating speed. A method of enhancing carrier mobility that has become a focus of recent attention is the use of silicon material to which a tensile strain is applied. "Strained" silicon may be formed by growing a layer of silicon on a silicon germanium substrate. The silicon germanium lattice is more widely spaced on average than a pure silicon lattice because of the presence of the larger germanium atoms in the lattice. Since the atoms of the silicon lattice align with the more widely spaced silicon germanium lattice, a tensile strain is created in the silicon layer. The silicon atoms are essentially pulled apart from one another. The amount of tensile strain applied to the silicon lattice increases with the proportion of germanium in the silicon germanium lattice.

[0008] The tensile strain applied to the silicon lattice increases carrier mobility. Relaxed silicon has six equal valence bands. The application of tensile strain to the silicon lattice causes four of the valence bands to increase in energy and two of the valence bands to decrease in energy. As a result of quantum effects, electrons effectively weigh 30 percent less when passing through the lower energy bands. Thus the lower energy bands offer less resistance to electron flow. In addition, electrons encounter less vibrational energy from the nucleus of the silicon atom, which causes them to scatter at a rate of 500 to 1000 times less than in relaxed silicon. As a result, carrier mobility is dramatically increased in strained silicon as compared to relaxed silicon, offering a potential increase in mobility of 80% or more for electrons and 20% or more for holes. The increase in mobility has been found to persist for current fields of up to 1.5 megavolts/centimeter. These factors are believed to enable a device speed increase of 35% without further reduction of device size, or a 25% reduction in power consumption without a reduction in performance.

[0009] An example of a MOSFET incorporating a strained silicon layer is shown in Figure 2. The MOSFET is fabricated on a substrate comprising a silicon germanium layer 32 grown on a silicon layer 10. An epitaxial layer of strained silicon 34 is grown on the silicon germanium layer 32. The MOSFET uses conventional MOSFET structures including deep source and drain regions 20, shallow source and drain extensions 28, a gate oxide layer 18, a gate 14 surrounded by a protective layer 30, a spacer 22, source and drain silicides 24, a gate silicide 26, and shallow trench isolations 12. The channel region of the MOSFET includes the strained silicon material, which provides enhanced carrier mobility between the source and drain.

[0010] An alternative to the formation of devices in semiconductor substrates is silicon on insulator (SOI) construction. In SOI construction, MOSFETs are formed on a substrate that includes a layer of a dielectric material beneath the MOSFET active regions. SOI devices have a number of advantages over devices formed in a shared semiconductor substrate, such as better isolation between devices, reduced leakage current, reduced latch-up between

CMOS elements, reduced chip capacitance, and reduction or elimination of short channel coupling between source and drain regions.

[0011] Figure 3 shows an example of a strained silicon MOSFET formed on an SOI substrate. In this example, the MOSFET is formed on an SOI substrate that comprises a silicon germanium layer 32 provided on a dielectric layer 36. The MOSFET is formed within an active region defined by trench isolations 12 that extend through the silicon germanium layer 32 to the underlying dielectric layer 36. In one alternative to the SOI structure of Figure 3, strained silicon FinFETs comprised of monolithic silicon germanium FinFET bodies having strained silicon grown thereon may be formed from the silicon germanium SOI substrate. An alternative type of SOI MOSFET, known as a FinFET, is formed by patterning monolithic semiconductor bodies comprising source, drain and channel regions from a semiconductor layer formed on a dielectric substrate.

[0012] The substrate for a conventional SOI device may be formed in a variety of manners. Figures 4a - 4b show structures formed using a buried oxide (BOX) method for forming an SOI substrate. As shown in Figure 4a, a silicon substrate 40 is provided. The silicon substrate 40 is implanted with oxygen 42 at an energy sufficient to form an oxygenated region 44 at such a depth as to leave a required thickness of silicon above the oxygenated region. Figure 4b shows the structure of Figure 4a after annealing of the silicon substrate 40 to form a buried silicon oxide layer 46 within the substrate. Annealing is typically performed at approximately 1350 degrees C for approximately four hours. The oxide layer 30 serves as the dielectric layer of the SOI substrate.

[0013] Figures 5a - 5d show structures formed in accordance with a wafer bonding method for forming an SOI substrate. Figure 5a shows a planarized silicon substrate 48. The substrate 48 is implanted with hydrogen 50 to form a hydrogen rich region 52 within the silicon material. The hydrogen 50 is implanted with an energy such that the amount of silicon remaining above the hydrogen rich region exceeds the thickness of the silicon layer to be formed on the SOI substrate. In some applications a different material such as oxygen may be implanted.

[0014] Figure 5b shows the silicon substrate 48 of Figure 5a after being cleaned, stripped of oxide in a diluted HF solution, rinsed in deionized water to form an active native oxide on its surface, and then inverted and bonded to a planarized oxide layer 56 formed on a semiconductor layer 58 of second substrate 54. To facilitate bonding, adjoining surfaces of the substrates are planarized to a homogeneity of 0.5 microns or less. Bonding is generally performed in two stages. In a first stage, the substrates are heated to approximately 600 degrees C in an inert environment for approximately three hours. As shown in Figure 5c, the heating of the first stage causes bonding of the silicon substrate 48 to the dielectric layer 56 of the second substrate 54 due to Van der Waals forces. The heating of the first stage also causes the first substrate 48 to fracture in the hydrogen rich region 52. After the first heating stage the fractured portion of the first substrate is removed, leaving a new substrate comprising a silicon layer 59 bonded to an oxide layer 56, and having a residual hydrogen rich region 52 at its upper surface.

[0015] In a second stage of the bonding process, the bonded structure is heated to approximately 1050 - 1200 degrees C for 30 minutes to two hours to strengthen the bond between the dielectric layer 56 and the silicon layer 59. The resulting substrate is then planarized and cleaned, leaving a silicon SOI substrate as shown in Figure 5d. Where it is desired to form strained silicon SOI devices, a silicon germanium SOI substrate may be formed instead of a silicon SOI substrate, and strained silicon may then be grown on the silicon germanium.

[0016] One detrimental property of strained silicon devices and SOI devices is that they have poor thermal conductivity compared to conventional devices formed in silicon substrates. Heat generated in the active region of a MOSFET formed in a silicon substrate is conducted away from the active region through the silicon substrate, which has a relatively good thermal conductivity of 1.5 W/cm-C°. In contrast, the thermal conductivity of a typical silicon germanium layer used in a strained silicon device is approximately 0.1 W/cm-C° for a silicon germanium layer having a 20% germanium content, which results in significantly less efficient dissipation of heat to the underlying silicon layer. Further, the oxide layer of an SOI substrate has a very poor thermal conductivity

of less than 0.02 W/cm-C°. As a result, insufficient dissipation of thermal energy can occur in strained silicon devices and particularly in strained silicon SOI devices, leading to significant self-heating. Self-heating is known to degrade the I-V characteristics of the MOSFET, such that a reduced source-drain current Ids is produced for a given source-drain voltage Vds.

[0017] Therefore the advantages of strained silicon MOSFETs and MOSFETs formed by SOI construction are partly offset by the disadvantages resulting from the poor thermal conductivity of silicon germanium and oxide layers.

SUMMARY OF THE INVENTION

In accordance with the invention, the thermal conductivity of strained silicon MOSFETs and strained silicon SOI MOSFETs is improved by providing a silicon germanium carbide thermal dissipation layer beneath a silicon germanium layer on which strained silicon is grown. The thermal conductivity of the silicon germanium carbide thermal dissipation layer depends on the proportion of carbon and may be in the range of 1 - 100 W/cm-C°. Thus the thermal conductivity of the silicon germanium carbide thermal dissipation layer is at least comparable to the thermal conductivity of silicon and may be significantly greater than the thermal conductivity of silicon where a large proportion of carbon is employed. Consequently the use of a silicon germanium carbide thermal dissipation layer improves the efficiency of the removal of thermal energy from the active regions of strained silicon devices.

[0018] In accordance with one embodiment of the invention, a MOSFET is formed on a substrate that comprises a layer of silicon germanium formed over a silicon germanium carbide thermal dissipation layer. The MOSFET typically is formed in an active region defined by shallow trench isolations, and includes strained silicon in at least the channel region. The substrate may be a semiconductor substrate in which the silicon germanium carbide thermal dissipation layer is formed on a silicon wafer, or the substrate may be an SOI substrate in which the silicon germanium carbide thermal dissipation layer is formed on a dielectric layer. The silicon germanium carbide thermal dissipation

layer provides enhanced thermal dissipation in both semiconductor substrate and SOI devices.

[0019] In accordance with further embodiments of the invention, a semiconductor device is fabricated by providing a substrate that comprises a silicon layer, a silicon germanium carbide thermal dissipation layer, and a silicon germanium layer. A layer of strained silicon is grown on the silicon germanium layer, and a MOSFET that incorporates the strained silicon in at least its channel region is then formed. Devices formed in this manner exhibit improved thermal dissipation compared to strained silicon MOSFETs formed on conventional silicon germanium substrates.

[0020] In accordance with further embodiments of the invention, a semiconductor device is fabricated by providing a substrate that comprises a dielectric layer, a silicon germanium carbide thermal dissipation layer, and a silicon germanium layer. A layer of strained silicon is grown on the silicon germanium layer, and then a MOSFET that incorporates the strained silicon in at least its channel region is formed on the substrate. The dielectric layer of the substrate may be formed by a buried oxide method or a wafer bonding method. Devices formed in this manner exhibit improved thermal dissipation compared to strained silicon SOI MOSFETs formed on silicon germanium SOI substrates.

DESCRIPTION OF THE DRAWINGS

[0021] Embodiments of the invention are described in conjunction with the following drawings, in which:

[0022] Figure 1 shows a conventional MOSFET formed in accordance with conventional processing;

[0023] Figure 2 shows a strained silicon MOSFET device;

[0024] Figure 3 shows a strained silicon MOSFET device formed on an SOI substrate;

[0025] Figures 4a and 4b show the formation of a buried oxide (BOX) SOI substrate;

[0026] Figures 5a, 5b, 5c and 5d show the formation of a SOI substrate by a wafer bonding method;

[0027] Figures 6a, 6b, 6c, 6d, 6e, 6f, 6g, 6h, 6i and 6j show structures formed during production of a MOSFET device in accordance with a first preferred embodiment of the invention;

[0028] Figures 7a and 7b show structures formed during production of a SOI substrate by a BOX method in accordance with a second preferred embodiment;

[0029] Figures 8a, 8b, 8c and 8d show structures formed during production of a SOI substrate by a wafer bonding method in accordance with the second preferred embodiment;

[0030] Figure 9 shows a process flow encompassing the first preferred embodiment and alternative embodiments; and

[0031] Figure 10 shows a process flow encompassing the second preferred embodiment and alternative embodiments.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0032] Figures 6a - 6j show structures formed during fabrication of a strained silicon SOI MOSFET in accordance with preferred embodiments of the invention. Figure 6a shows a structure comprising a silicon substrate 10 having grown thereon a silicon germanium carbide thermal dissipation layer 60, and having a silicon germanium layer 62 grown on the thermal dissipation layer 60.

[0033] The silicon germanium carbide thermal dissipation layer 60 preferably has a lattice constant that is matched to the lattice constant of the overlying silicon germanium layer. In general the composition of the silicon germanium carbide layer is 60 - 90% silicon, 10 - 40% germanium, and 10 - 30% carbon, with increased proportions of silicon and carbon providing increased thermal conductivity. Silicon germanium carbide may be grown, for example, by chemical vapor deposition using source gases including a silicon source gas such as Si_2H_6 (disilane) or SiH_4 (silane), a germanium source gas such as GeH_4 (germane), and a carbon source gas such as methane (CH_4). In the alternative, an organosilane source gas may provide both silicon and carbon precursors. Such gases include methylsilane ($SiCH_6$), dimethylsilane (SiC_2H_8), trimethylsilane (SiC_3H_{10}), tetramethylsilane (SiC_4H_{12}), and diethylsilane (SiC_4H_{12}).

A typical deposition temperature is in the range of 200 - 700 degrees C, and pressures and flow rates for the gases are selected in accordance with the particular composition to be produced. The entire thickness of the silicon germanium carbide thermal dissipation layer 62 may be grown with uniform proportions, or alternatively the partial pressure of GeH_4 may be gradually increased beginning from a lower pressure or zero pressure to form a gradient composition having a high silicon carbide content and a low germanium content at the lower portion, and a higher germanium content at the upper portion. The thickness of the silicon germanium carbide thermal dissipation layer 60 may be determined in accordance with the particular application.

[0034] The silicon germanium layer 62 preferably has a composition $Si_{1-x}Ge_x$, where x is approximately 0.2, and is more generally in the range of 0.1 to 0.3. Silicon germanium may be grown, for example, by chemical vapor deposition using Si_2H_6 (disilane) and GeH_4 (germane) as source gases, with a substrate temperature of 600 to 900 degrees C, a Si_2H_6 partial pressure of 30 mPa, and a GeH_4 partial pressure of 60 mPa. SiH_4 (silane) may be used as a source of silicon in alternative processes. The upper portion of the silicon germanium substrate 62 should have a uniform composition. The silicon germanium carbide layer 60 and the silicon germanium layer 62 are preferably grown in a single continuous in situ deposition.

[0035] Figure 6b shows the structure of Figure 6a after formation of shallow trench isolations 66 having tapered sidewalls in the silicon germanium layer 62, followed by selective growth of an epitaxial layer of strained silicon layer 64 on the silicon germanium layer 62. The shallow trench isolations 44 define an active region of the substrate in which a MOSFET will be formed. The shallow trench isolations 66 may be formed by forming trenches in the silicon germanium, performing a brief thermal oxidation of the silicon germanium, and then depositing a layer of silicon oxide to a thickness that is sufficient to fill the trenches, such as by low pressure CVD (LPCVD) TEOS or atmospheric pressure ozone TEOS. The silicon oxide layer is then densified and planarized such as by chemical mechanical polishing or an etch back process. In accordance with one preferred alternative, the shallow trench isolations are comprised of an oxide

trench liner and a silicon carbide bulk fill material. The silicon carbide bulk fill material has high thermal conductivity and provides further dissipation of heat generated in the active regions. Shallow trench isolations of this type preferably contact the silicon germanium carbide layer to provide a direct path for thermal dissipation.

[0036] The strained silicon layer 64 is preferably grown by chemical vapor deposition using Si_2H_6 as a source gas with a partial pressure of 30mPa and a substrate temperature of approximately 600 to 900 degrees C. The strained silicon layer is preferably grown to a thickness of 200 Angstroms. The maximum thickness of strained silicon that can be grown without misfit dislocations will depend on the percentage of germanium in the silicon germanium layer 62. It is preferable to form the shallow trench isolations 66 prior to growth of the strained silicon layer 64 to avoid creation of misfit dislocations in the strained silicon 64 as a result of the high temperatures used during formation of the shallow trench isolations.

[0037] Figure 6c shows the structure of Figure 6b after formation of multiple layers of material over the strained silicon layer 64 and the shallow trench isolations 66. A thin gate insulating layer 68 is formed on the strained silicon layer 64. The gate insulating layer 68 is typically silicon oxide but may be another material such as silicon oxynitride. Silicon oxide may be grown by thermal oxidation of the strained silicon layer 64 or may be deposited by chemical vapor deposition. Formed over the gate insulating layer 68 is a gate conductive layer 70. The gate conductive layer 70 typically comprises polysilicon that is heavily doped with an n-type dopant such as arsenic or boron. In some instances the polysilicon may also be implanted with germanium to create strain for enhancing carrier mobility. Overlying the gate conductive layer 70 is a bi-layer hardmask structure comprising a lower hardmask layer 72, also referred to as a bottom antireflective coating (BARC), and an upper hardmask layer 74. The lower hardmask layer 72 is typically silicon oxynitride and the upper hardmask layer 74 is typically silicon nitride (e.g. Si_3N_4). The thicknesses of the layers are chosen to provide the desired antireflective properties.

[0038] Figure 6d shows the structure of Figure 6c after patterning of the gate conductive layer to form a gate 76. Patterning of the gate conductive layer typically removes at least a portion of any unprotected gate insulator layer material, leaving a gate insulator 78 beneath the gate 76. Patterning is performed using a series of anisotropic etches that patterns the upper hardmask layer using a photoresist mask as an etch mask, then patterns the lower hardmask layer using the patterned upper hardmask layer as an etch mask, then patterns the polysilicon using the patterned lower hardmask layer as an etch mask. A protective cap 80 formed from the silicon oxynitride BARC layer may be left on the gate 76.

[0039] Figure 6e shows the structure of Figure 6d after formation of a protective silicon oxide layer 82 on the strained silicon layer 64 and the exposed sidewalls of the gate 76. The protective layer 82 may be formed by thermal oxidation of the gate 76 and strained silicon 64.

[0040] Figure 6f shows the structure of Figure 6e after implantation of dopant by ion implantation to form shallow source and drain extensions 84 in the strained silicon layer 64 and silicon germanium layer 62 at opposing sides of the gate 76. Halo regions (not shown) may be implanted prior to implantation of the shallow source and drain extensions 84. Halo regions are regions that are implanted with a dopant that has a conductivity type that is opposite to that of the source and drain region dopants. The dopant of the halo regions retards diffusion of the dopant of the source and drain extensions. Halo regions are preferably implanted using a low energy at an angle to the surface of the substrate so that the halo regions extend beneath the gate 76 to beyond the anticipated locations of the ends of the source and drain extensions 84 after annealing.

[0041] Figure 6g shows the structure of Figure 6f after formation of a spacer 86 around the gate 76. The spacer 86 is preferably formed of silicon oxide. The spacer 86 may be formed by depositing a conformal layer of silicon oxide, followed by an etch back process to remove the silicon oxide from the substrate, leaving silicon oxide on the sidewalls of the gate as the spacer 80.

[0042] Figure 6h shows the structure of Figure 6g after formation of deep source and drain regions 88 in the strained silicon 64 and silicon germanium 62 layers at opposing sides of the gate 76 by implantation of dopant. The spacer 86 serves as a mask during implantation of the deep source and drain regions 88 to define the lateral positions of the source and drain regions 88 relative to the gate 76.

[0043] Figure 6i shows the structure of Figure 6h after performing rapid thermal annealing (RTA) to anneal the silicon germanium layer 62 and strained silicon layer 64 and to activate the dopants implanted in the shallow source and drain extensions 84 and the deep source and drain regions 88. During annealing the implanted dopant undergoes diffusion, causing a smoothing of the contours of the respective regions.

[0044] Figure 6j shows the structure of Figure 6i after formation of source and drain silicides 90 and a gate silicide 92. The silicides 90, 92 are formed of a compound comprising a semiconductor material and a metal. Typically a metal such as cobalt (Co) is used, however other metals such as nickel (Ni) may also be employed. The silicides are formed by depositing a thin conformal layer of the metal over the entire structure, and then annealing to promote silicide formation at the points of contact between the metal and underlying semiconductor materials, followed by stripping of residual metal. Formation of silicides is typically preceded by a patterning step to remove oxides and protective layers from portions of the gate and the source and drain regions where the silicides are to be formed.

[0045] The structure of Figure 6j is advantageous compared to the conventional structure of Figure 2 in that the silicon germanium carbide thermal dissipation layer 60 conducts heat away from the active regions to the silicon substrate more efficiently than the silicon germanium layer of the conventional device, thus reducing self heating and improving device performance.

[0046] Figure 9 shows a process flow for forming a semiconductor device encompassing the preferred embodiment of Figures 6a - 6j and alternative embodiments. Initially a substrate is provided (120). The substrate comprises a silicon layer, a silicon germanium carbide thermal dissipation layer, and a silicon

germanium layer. A layer of strained silicon is then grown on the silicon germanium layer (122), and a MOSFET that incorporates the strained silicon in at least its channel region is then formed (124).

[0047] While the structures illustrated in Figures 6a - 6j represent processing performed in accordance with one preferred embodiment of the invention, a variety of alternatives may be implemented. For instance, a silicon germanium carbide thermal dissipation layer may be implemented in an SOI substrate that includes a silicon germanium layer for the formation of strained silicon. Such a substrate may be formed using either a buried oxide (BOX) method or a bonding method.

[0048] Figures 7a - 7b show structures formed during processing to produce an SOI substrate comprising a silicon germanium carbide thermal dissipation layer using the buried oxide (BOX) method. As shown in Figure 7, a substrate including a silicon layer 94, a silicon germanium carbide layer 96 and a silicon germanium layer 98 is provided. This structure may be fabricated as described above with respect to Figure 6a. Oxygen 100 is implanted into the silicon germanium carbide layer 96 to form an oxygen implanted region 102. The substrate is then annealed to form an oxide layer 103 within the silicon germanium carbide layer 96 as shown in Figure 7b. MOSFETs may then be formed on this substrate, for example using the processing illustrated in Figures 6a-6j. The processing of Figures 7a - 7b is preferred in that forms the buried oxide layer prior to growth of strained silicon, thereby avoiding the creation of misfit dislocations in the strained silicon that would occur when subjected to the high temperatures used for oxide formation.

[0049] Figures 8a - 8d shows structures formed during processing to produce an SOI substrate comprising a silicon germanium carbide thermal dissipation layer using the wafer bonding method. Figure 8a shows a first silicon substrate 104 having formed thereon a silicon germanium layer 106 and a silicon germanium carbide layer 108. The first substrate 104 is implanted with hydrogen 110 to form a hydrogen rich region 112 within the silicon germanium layer 106. The hydrogen 110 is implanted with an energy such that the amount of silicon germanium remaining above the hydrogen rich region

exceeds the thickness of the silicon germanium layer to be formed on the SOI substrate. In some applications a different material such as oxygen may be implanted.

[0050] Figure 8b shows the silicon substrate 104 of Figure 8a after being cleaned, stripped of oxide in a diluted HF solution, rinsed in deionized water to form an active native oxide on its surface, and then inverted and bonded to a planarized dielectric layer 114 formed on a semiconductor layer of second substrate 116. The second substrate 116 is typically a silicon wafer and the dielectric layer 114 is typically a silicon oxide layer. To facilitate bonding, the substrates should be planarized to a homogeneity of 0.5 microns or less. Bonding is generally performed in two stages. In a first stage, the substrates are heated to approximately 600 degrees C in an inert environment for approximately three hours. As shown in Figure 8c, the heating of the first stage causes the silicon germanium carbide layer 108 of the first substrate to bond to the dielectric layer 114 of the second substrate by means of Van der Waals forces. This heating also causes the silicon germanium layer 106 of the first substrate to fracture in the hydrogen rich region 112, thus yielding a new substrate comprising a silicon germanium carbide layer 108 bonded to an oxide layer 114, and having a silicon germanium layer 106 formed thereon and a residual hydrogen rich region 112 at the upper surface of the silicon germanium layer 106. In a second stage of the bonding process, the bonded structure is heated to approximately 1050 - 1200 degrees C for 30 minutes to two hours to strengthen the bond between the dielectric layer 114 and the silicon germanium carbide layer 108.

[0051] The resulting substrate is then planarized and cleaned, leaving a silicon germanium SOI substrate having a silicon germanium carbide thermal dissipation layer 108 overlying a dielectric layer 114 as shown in Figure 5d.

[0052] While the aforementioned SOI substrate fabrication processes use a silicon germanium carbide thermal dissipation layer that is grown in situ in a single continuous process with a silicon germanium layer, the silicon germanium carbide layer may be formed in other manners. For example, the layer may be formed by growing a silicon germanium layer and then implanting carbon at an

appropriate depth and in an appropriate dose, followed by annealing to form the desired silicon germanium carbide compound. In another alternative, a silicon germanium layer may be grown and carbon may then be diffused into the silicon germanium using a suitable precursor. An additional silicon germanium layer may then be grown over the silicon germanium carbide.

[0053] Figure 10 shows a process flow for forming a semiconductor device encompassing the preferred embodiments of Figures 7a-7b and 8a-8d and alternative embodiments. Initially a substrate is provided (130). The substrate comprises a dielectric layer, a silicon germanium carbide thermal dissipation layer, and a silicon germanium layer. The substrate may be formed by a buried oxide method or a wafer bonding method. A layer of strained silicon is then grown on the silicon germanium layer (132), and a MOSFET that incorporates the strained silicon in at least its channel region is then formed on the substrate (134).

[0054] A variety of embodiments may therefore be implemented in accordance with the invention. In general terms, embodiments of the invention are implemented as strained silicon MOSFETs formed on a substrate comprising a layer of silicon germanium formed over a silicon germanium carbide thermal dissipation layer. The MOSFETs typically include strained silicon in at least their channel regions. The MOSFETs are typically formed in active regions of the substrate defined by shallow trench isolations. The substrate may be a semiconductor substrate in which the silicon germanium carbide thermal dissipation layer is formed on a silicon wafer, or the substrate may be an SOI substrate in which the silicon germanium carbide thermal dissipation layer is formed on a dielectric layer. The silicon germanium carbide thermal dissipation layer provides enhanced thermal dissipation in both semiconductor substrate and SOI devices.

[0055] It may be desirable to implement other features in order to further improve device performance. For example, source and drain silicides may be formed using a metal that produces a silicide having an inherent compressive strain. The resulting compression in the source and drain silicides applies tensile strain to the channel region, thus further enhancing channel region carrier

mobility. Topside passivation materials may also be chosen to induce further strain in the strained silicon. It may also be desirable to remove the silicon germanium material beneath the strained silicon of the channel region to leave an open cavity, thus effectively creating a fully depleted strained silicon on insulator channel region.

[0056] The tasks described in the above processes are not necessarily exclusive of other tasks, and further tasks may be incorporated into the above processes in accordance with the particular structures to be formed. For example, intermediate processing tasks such as formation and removal of passivation layers or protective layers between processing tasks, formation and removal of photoresist masks and other masking layers, doping and counter-doping, cleaning, planarization, and other tasks, may be performed along with the tasks specifically described above. Further, the processes described herein need not be performed on an entire substrate such as an entire wafer, but may instead be performed selectively on sections of the substrate. Also, while tasks performed during the fabrication of structure described herein are shown as occurring in a particular order for purposes of example, in some instances the tasks may be performed in alternative orders while still achieving the purpose of the process. Thus, while the embodiments illustrated in the figures and described above are presently preferred, it should be understood that these embodiments are offered by way of example only. The invention is not limited to a particular embodiment, but extends to various modifications, combinations, and permutations that fall within the scope of the claimed inventions and their equivalents.